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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,025	01/30/2004	Zhong Dong	M-12327-3C US	7632

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MACPHERSON KWOK CHEN & HEID LLP
1762 TECHNOLOGY DRIVE, SUITE 226
SAN JOSE, CA 95110

EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,025	DONG ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 10-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 10-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Attorney's Docket Number: M-12327-3C US
Filing Date: 1/30/2004
Claimed Priority Date: 2/8/2002 (Continuation of 10/071,689)
Applicant(s): Dong, et al.
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the response filed on 4/18/2005.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-3, 10, 12-21, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 6127227), Misium (US 6261973), and George (US 6140024).

4. Regarding claim 1, Lin shows most aspects of the instant invention including a method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

- Forming a conductive first layer **120** containing primarily silicon, the first layer providing one or more floating gates for the memory (see, *e.g.*, fig. 2B)
- Nitriding a silicon-containing surface of the first layer **120** to incorporate nitrogen atoms into the silicon-containing surface of the first layer (see, *e.g.*, fig. 2B)
- Subjecting the nitrided surface **124** to a thermally oxidizing atmosphere so as to thereby form a thermally-grown silicon oxide **143** at the nitrided surface **125**, the combination of the thermally-grown silicon oxide and incorporated nitrogen atoms defining at least part of a first dielectric **140** of the memory
- Forming a conductive second layer **150** separated from the conductive material of the first layer **120** by the first dielectric **140**, the conductive second layer **150** providing one or more control gates for the memory

Lin (see, *e.g.*, col.4/ll.39-46) also teaches that a nitrogen treatment or ion implantation may be used during the nitriding step to incorporate nitrogen atoms into the silicon surface, but fails to specify the use of a low temperature, low energy, surface nitriding process such as remote plasma nitridation (RPN).

Misium (see, *e.g.*, col.2/ll.1-3), on the other hand, teaches that RPN is an improved low-temperature ion-implantation step that can be used for creating Lin's nitrided layer. This method step will help prevent device failure due to the mechanical

stress occurring within nitride layers during high-temperature processing steps (see, *e.g.*, col.1/ll.63-67). In addition, Misium teaches that RPN may be used during the nitridation step of either an oxide layer (see, *e.g.*, figs. 1C and 2B) or a silicon surface (see, *e.g.*, fig. 3C).

Likewise, George (see, *e.g.*, col.2/ll.21-33) teaches that using RPN for nitriding an oxide layer will help lessen the usual stress associated with nitride layers while providing for a low-temperature nitriding step. George further teaches that RPN may also be used to protect the silicon surface of Lin's first conductive layer (see, *e.g.*, col.5/ll.62-67). Doing so will improve the device reliability (see, *e.g.*, col.5/ll.67-col.6/ll.2).

It would have been obvious at the time of the invention to one of ordinary skill in the art to nitride Lin's first conductive layer by RPN, as suggested by Misium and George, to lower the thermal budget of the process and improve the device reliability.

5. Regarding claim 2, Lin shows that the step of forming the silicon oxide at the nitrided surface comprises performing oxidation at a temperature in the range of 800°C-1050°C in an oxygen or oxygen/hydrogen atmosphere to thereby form the silicon oxide by thermal oxidation (see, *e.g.*, col.4/ll.61).

6. Regarding claim 3, Lin shows that the surface of the first layer is a polysilicon surface (see, *e.g.*, col.4/ll.29).

7. Regarding claim 10, George (see, *e.g.*, col.5/ll.62-67) and Misium (see, *e.g.*, fig. 3C) use an RPN process for the nitriding step.

8. Regarding claim 12, Lin teaches that the nitriding step provides a nitrided surface having a composition of nitrogen, oxygen and silicon atoms (see, *e.g.*, col.4/ll.62-65), but fails to specify the concentration of nitrogen atoms within said composition. However, differences in concentration will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration is critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

The specific claimed nitrogen concentrations, *i.e.*, 1-20 at%, absent any criticality, are only considered to be the "optimum" concentrations disclosed by Lin that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained as long as a nitrided surface of a first conductive layer is used, as already suggested by Lin.

Accordingly, since the applicants have not established the criticality (see next paragraph below) of the stated concentrations, it would have been obvious to one of ordinary skill in the art to use these values in the device of Lin/Misium/George.

CRITICALITY

9. The specification contains no disclosure of either the critical nature of the claimed concentrations or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

10. Regarding claim 13, Lin (see, *e.g.*, col.4/ll.66) shows that nitriding step results in incorporating the nitrogen atoms to a depth of no more than 3 nm into the first layer.

11. Regarding claim 14, Lin shows that the first layer **120** is disposed over a tunneling dielectric **110** (see, *e.g.*, fig. 2B).

12. Regarding claim 15, Lin shows the method further comprising thermally growing the tunneling dielectric (see, *e.g.*, col.4/ll.25).

13. Regarding claim 16, Lin shows (see, *e.g.*, fig. 2D) the method further comprising the step of depositing a silicon nitride layer **145** on the combination of the thermally-grown silicon oxide and incorporated nitrogen atoms to thereby define a further part of the first dielectric **140** of the memory.

14. Regarding claim 17, Lin shows (see, *e.g.*, fig. 2E) the method further comprising a step of depositing a silicon oxide layer **147** on the deposited silicon nitride layer **145** to thereby define a yet further part of the first dielectric **140** of the memory.

15. Regarding claim 18, Lin shows most aspects of the instant invention including a method of manufacturing a nonvolatile memory cell within a monolithically integrated circuit, the method comprising:

- Forming a tunneling dielectric layer **110** on a semiconductive substrate **100** (see, *e.g.*, fig. 2A)
- Forming a floating gate layer **120** on the tunneling layer **110**, the floating gate layer **120** having a top surface composed primarily of conductive silicon

- Surface nitriding the top surface of the floating gate layer **120** so as to incorporate nitrogen atoms into the top surface **125** of the floating gate layer **120** (see, *e.g.*, fig. 2B)
- Subjecting the nitrided top surface **125** to a thermally oxidizing atmosphere so as to thereby form a combination of thermally-grown silicon oxide and surface incorporated and thermally treated nitrogen atoms at the nitrided and thermally oxidized top surface of the floating gate layer **120** (see, *e.g.*, col.4/ll.55-65)

Lin (see, *e.g.*, col.4/ll.39-46) also teaches that a nitrogen treatment or ion implantation may be used during the nitriding step to incorporate nitrogen atoms into the silicon surface, but fails to specify the use of a low temperature, low energy, surface nitriding process such as remote plasma nitridation (RPN).

Misium (see, *e.g.*, col.2/ll.1-3), on the other hand, teaches that RPN is an improved low-temperature ion-implantation step that can be used for creating Lin's nitrided layer. This method step will help prevent device failure due to the mechanical stress occurring within nitride layers during high-temperature processing steps (see, *e.g.*, col.1/ll.63-67). In addition, Misium teaches that RPN may be used during the nitridation step of either an oxide layer (see, *e.g.*, figs. 1C and 2B) or a silicon surface (see, *e.g.*, fig. 3C).

Likewise, George (see, *e.g.*, col.2/ll.21-33) teaches that using RPN for nitriding an oxide layer will help lessen the usual stress associated with nitride layers while providing for a low-temperature nitriding step. George further teaches that RPN may

also be used to protect the silicon surface of Lin's first conductive layer (see, *e.g.*, col.5/ll.62-67). Doing so will improve the device reliability (see, *e.g.*, col.5/ll.67-col.6/ll.2).

It would have been obvious at the time of the invention to one of ordinary skill in the art to nitride Lin's silicon surface by RPN, as suggested by Misium and George, to lower the thermal budget of the process and improve the device reliability.

16. Regarding claim 19, Lin further shows a step of depositing a silicon nitride layer **145** directly on the nitrided and thermally oxidized top surface of the floating gate layer **120** (see, *e.g.*, fig. 2D).

17. Regarding claims 20 and 24, Lin further teaches that subjecting the nitrided top surface **125** to the thermally oxidizing atmosphere consumes at least silicon atoms from the nitrided top surface **125** to form thermally-grown silicon dioxide **143** at the top of the nitrided and thermally oxidized top surface (see, *e.g.*, col.4/ll.55-65 and fig. 2C).

18. Regarding claim 21, Lin further shows a step of depositing a silicon oxide layer **147** directly on the nitride layer **145** (see, *e.g.*, fig. 2E).

19. Regarding claim 25, Lin shows that the step of surface nitriding incorporates nitrogen atoms into the top surface of the floating gate layer to a depth of less than 3 nm (see, *e.g.*, col.4/ll.66).

20. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin/Misium/George in view of Zheng (US 6653199).

21. Regarding claim 11, Lin/Misium/George shows most aspects of the instant invention (see, *e.g.*, paragraphs 4-19 above). Misium (see, *e.g.*, fig. 3C) and George

(see, *e.g.*, col.5/ll.62-67), for example, use RPN during the step of nitriding the surface of the first conductive layer, but fail to teach the use of decoupled plasma nitridation (DPN). Zheng (see, *e.g.*, col.4/ll.57-60), on the other hand, teaches that DPN is an alternative equivalent technique to the use of RPN during the step of nitriding the first conductive layer.

It would have been obvious at the time of the invention to one of ordinary skill in the art to use either DPN or RPN, as taught by Zheng, during the nitridation step of Lin/Misium/George since the use in the semiconductor art of any of these known equivalent techniques for nitriding a conductive layer would have been within the level of ordinary skill in the art at the time of the invention.

22. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin/Misium/George in view of Hagiwara (US 5847427).

23. Regarding claim 22, Lin/Misium/George shows most aspects of the instant invention (see, *e.g.*, paragraphs 4-19 above), except for a step of nitridating the surface of the deposited silicon oxide layer so as to incorporate nitrogen atoms into the layer. Hagiwara (see, *e.g.*, col.7/ll.1-4), on the other hand, teaches that doing so would reduce the deterioration of the write/erase characteristics of the memory.

It would have been obvious at the time of the invention to one of ordinary skill in the art to incorporate a step of nitriding the surface of the deposited silicon oxide layer of Lin/Misium/George, as suggested by Hagiwara, to reduce the deterioration of the write/erase characteristics of the memory.

24. Regarding claim 23, Hagiwara (see, *e.g.*, fig. 13) forms a conductive gate layer **204** over the surface nitridated and deposited silicon oxide layer.

Response to Arguments

25. The applicants argue:

> Lin never mentions anything about using a surface nitriding process or about nitriding the surface of the first polysilicon layer. There is no surface nitridation in Lin. Instead the nitrogen treatment of Lin creates a nitrogen region at dashed line **25** with the thickness above the line being free of nitrogen. There is no nitridation extending from the surface to a given depth below the surface. The reason why Lin avoided mentioning that the surface of the polysilicon layer **120** is nitride would have been very clear to one of ordinary skill in the art. It is because the ion implantation technique that Lin teaches will result in the nitrogen ions being implanted at a given depth below the surface of the polysilicon layer **120**, thereby creating a buried nitride layer.

The examiner responds:

Lin lacks any teaching describing the region above line **25** as being free of nitrogen. On the contrary, Lin clearly teaches that nitrogen is present in the upper layers of the polysilicon layer **120**. The dashed line **125** is used to indicate the upper layers of the polysilicon layer **120** wherein the nitrogen is present (see, *e.g.*, col.4/ll.46-48). As seen in figure 2A the upper layers of the polysilicon layer **120** include its surface.

To support their saying that the region above line **125** is free of nitrogen, the applicants rely on the implantation technique used by Lin. According to the applicants, due to said implantation the nitrogen ions would be located below the surface. However, the applicants failed to notice that said technique is but one of the two processes disclosed by Lin. Lin is not restricted to said implantation technique. The surface of the polysilicon layer may also be subjected to a nitrogen treatment at a pressure between about 400 to 600 milliTorr (see, *e.g.*, col.4/ll.39-42).

26. The applicant argue:

There is no teaching or suggestion in either Misium or George that their nitriding methods can be used to form the buried nitride layer of Lin by RPN.

The examiner responds:

Regarding the buried layer, see comments stated above in paragraph 25, which are considered repeated here.

Regarding the teachings of Misium, see, *e.g.*, col.2/ll.1-3, where Misium clearly teaches that RPN is an improved low-temperature ion-implantation step that can be used for creating Lin's nitrided layer. This method step will help prevent device failure due to the mechanical stress occurring within nitride layers during high-temperature processing steps (see, *e.g.*, col.1/ll.63-67). In addition, Misium teaches that RPN may be used during the nitridation step of either an oxide layer (see, *e.g.*, figs. 1C and 2B) or a silicon surface (see, *e.g.*, fig. 3C).

Likewise, George (see, *e.g.*, col.2/ll.21-33) teaches that using RPN for nitriding an oxide layer will help lessen the usual stress associated with nitride layers while providing for a low-temperature nitriding step. George further teaches that RPN may also be used to protect the silicon surface of Lin's first conductive layer (see, *e.g.*, col.5/ll.62-67). Doing so will improve the device reliability (see, *e.g.*, col.5/ll.67-col.6/ll.2).

27. The applicants argue:

Woodruff does not stand for the preposition that an applicant must always show criticality. Applicants do not have to establish criticality until after the PTO has found art with subsuming or fully overlapping ranges. Only at that point where the PTO had demonstrated complete overlap of ranges did the burden shift to the applicant to submit rebuttal evidence of unexpected results.

The examiner responds:

In raising the issue of criticality the examiner considered all the relevant facts in the record. Firstly, the issue was raised since it was the applicants themselves who established the non-critical nature of the nitrogen surface concentration. See, *e.g.*, pp.4/ll.15-18 of the specification, where the applicants describe the range of 1-20 atomic percent as exemplary and not limiting. The examiner repeated applicants' own teachings about the non-criticality of the nitrogen concentration for the purpose of establishing a clear record. Secondly, the issue of criticality is properly raised whenever there are differences between the claimed invention and the prior art. In the instant case, and as explained above in paragraphs 8 and 25, Lin shows the presence of nitrogen in the nitrided surface but fails to specify the nitrogen concentration. Lastly, the issue of criticality was properly raised due to the fact that this range of nitrogen concentrations is commonly used in the semiconductor art, and due to the fact that the applicants indicated that said range was not critical to the invention and to the absence of any evidence to the contrary. See, *e.g.*, Ito (US 5650344/col.3.kk,61-63), Mogami (US 6459126/fig.10), and Halliyal (US 6721046/col.4/ll.38-40) as evidence that a nitrogen concentration between 1-20 atomic percent is common in the semiconductor art.

Conclusion

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

29. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

30. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 872-9306**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

32. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

33. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 438/257-267,514-534; 257/324	5/3/2005
Other Documentation: PLUS Analysis	3/10/2005
Electronic Database(s): EAST (USPAT, EPO, JPO)	5/3/2005

Marcos D. Pizarro-Crespo
Patent Examiner
Art Unit 2814
703-308-6558
marcos.pizarro@uspto.gov

Howard Weiss
Primary Examiner
Art Unit 2814

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